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(54) **NOISE DECOUPLING STRUCTURE WITH THROUGH-SUBSTRATE VIAS**

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(51) **Int. Cl.**

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H01L 23/58	(2006.01)
H01L 21/762	(2006.01)
H01L 21/768	(2006.01)
H01L 29/06	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/66*** (2013.01); ***H01L 21/76224*** (2013.01); ***H01L 21/76898*** (2013.01); ***H01L 23/585*** (2013.01); ***H01L 29/0619*** (2013.01); *H01L 2223/6616* (2013.01); *H01L 2223/6666* (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC ... H01L 23/481; H01L 23/585; H01L 23/552; H01L 23/64; H01L 23/66

See application file for complete search history.

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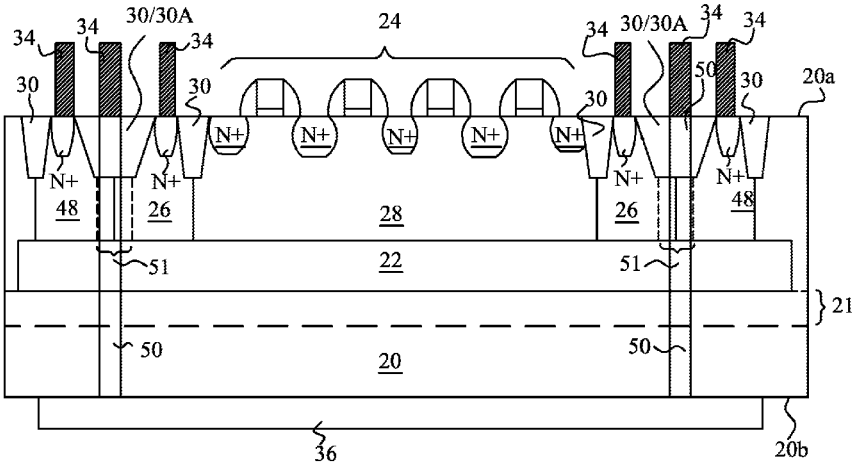
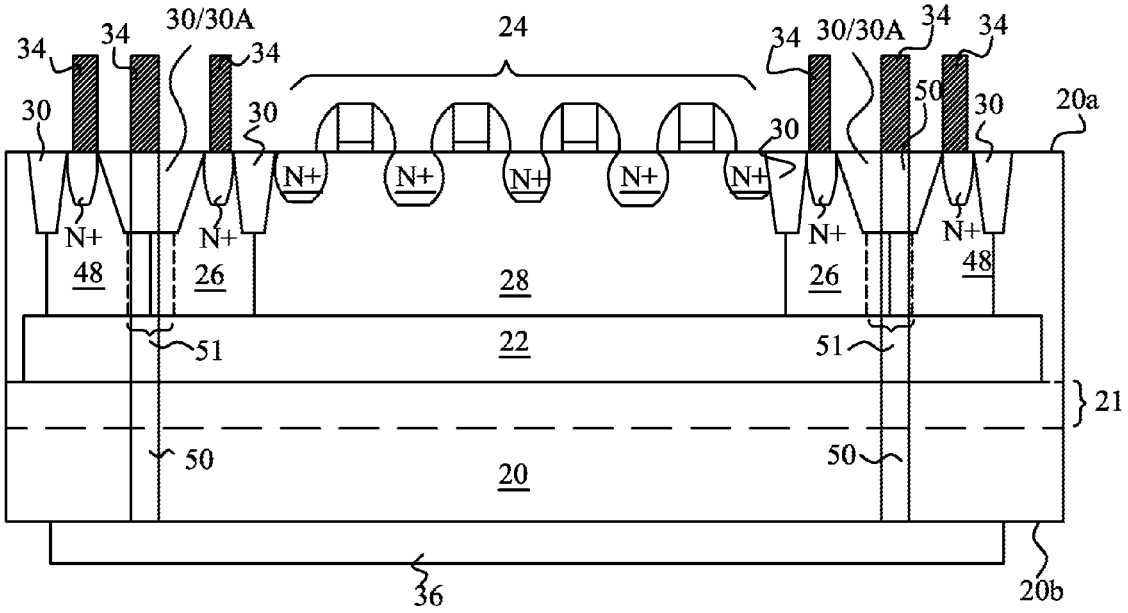
(57) **ABSTRACT**

A device includes a substrate having a front surface and a back surface; an integrated circuit device at the front surface of the substrate; and a metal plate on the back surface of the substrate, wherein the metal plate overlaps substantially an entirety of the integrated circuit device. A guard ring extends into the substrate and encircles the integrated circuit device. The guard ring is formed of a conductive material. A through substrate via (TSV) penetrates through the substrate and electrically couples to the metal plate.

20 Claims, 4 Drawing Sheets

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20b

Fig. 1A

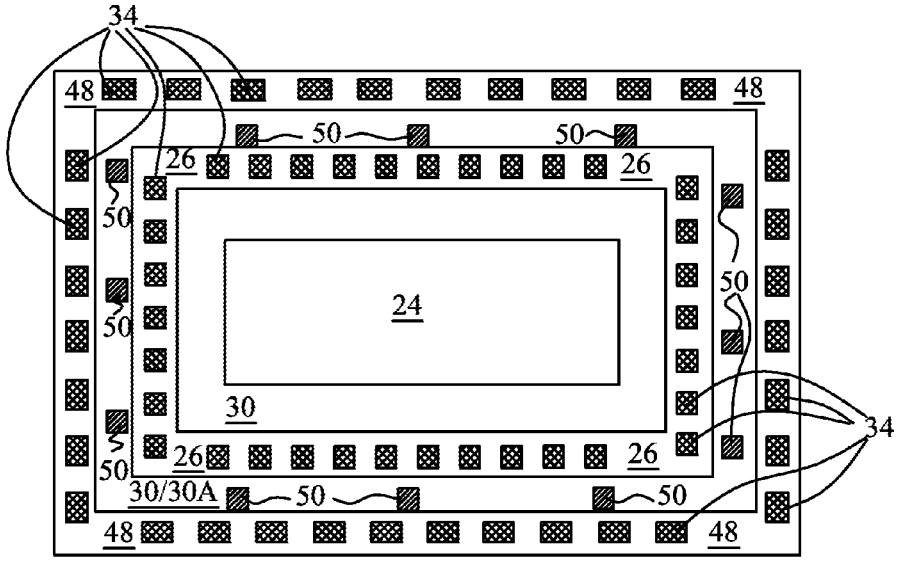
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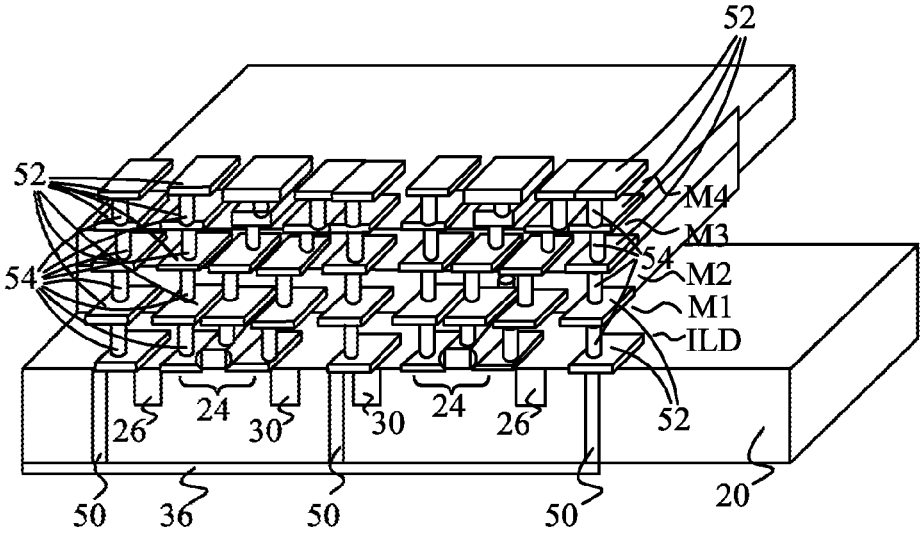
Fig. 1B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M4
M3
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M2
M1
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Fig. 1C

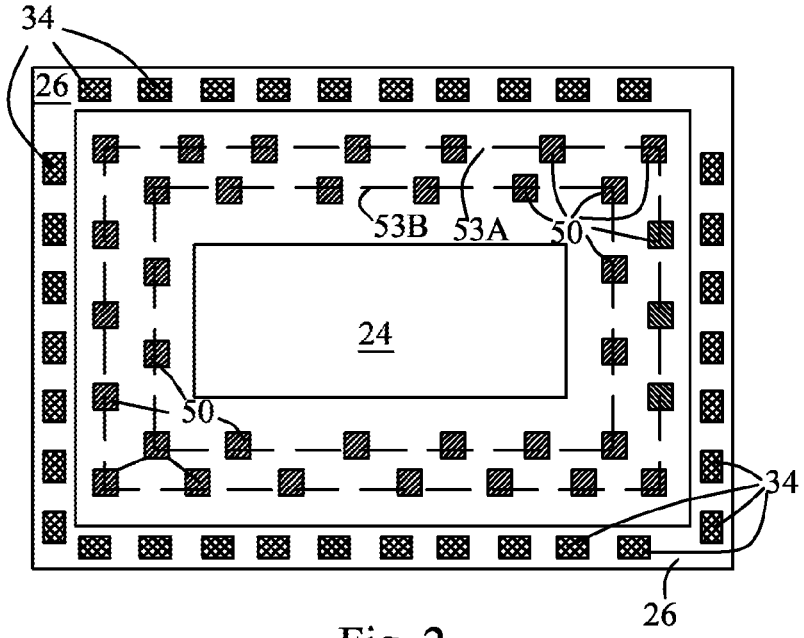
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Fig. 2

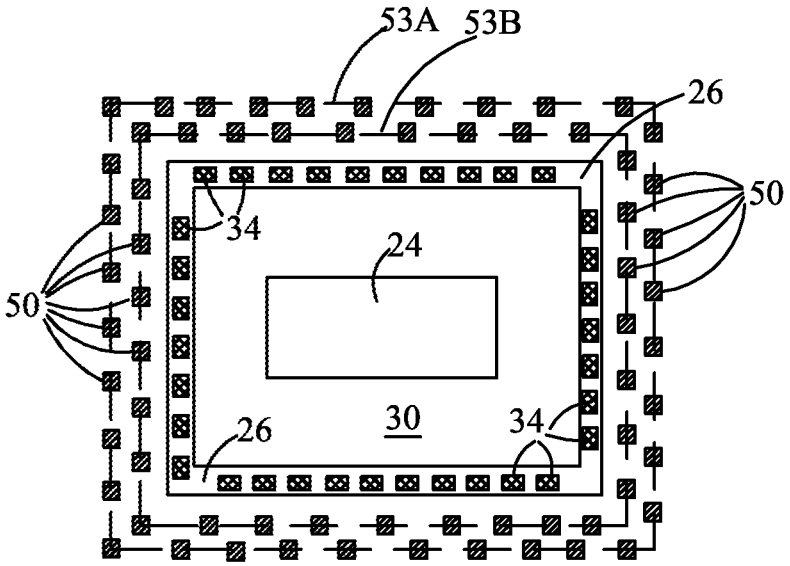

Fig. 3A

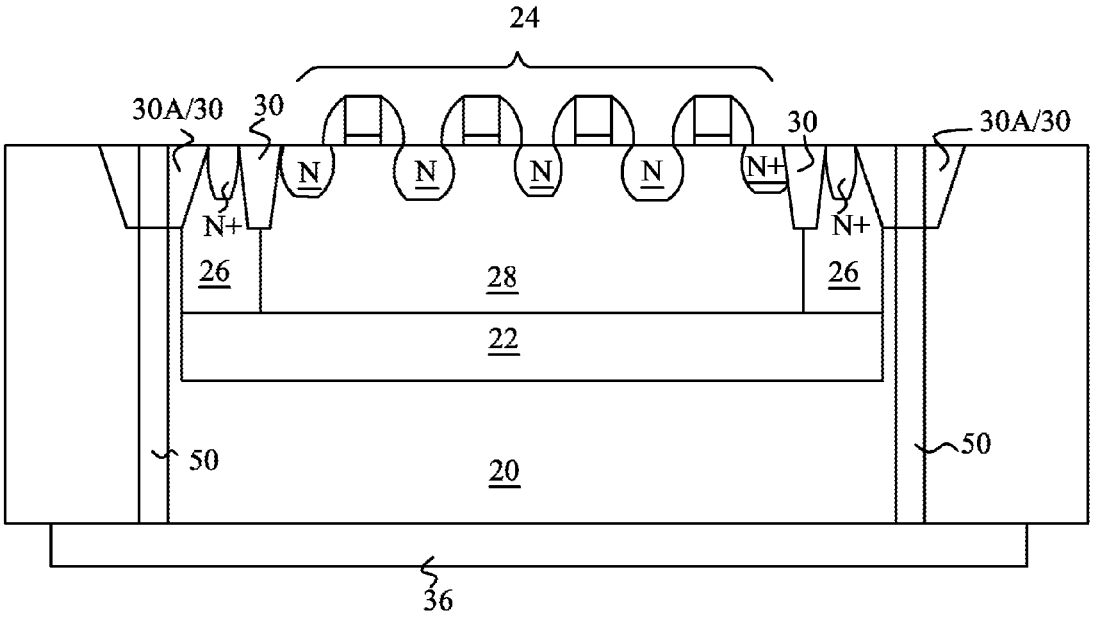

Fig. 3B

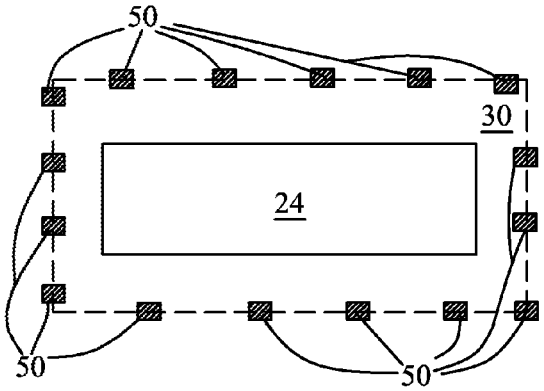

Fig. 4

NOISE DECOUPLING STRUCTURE WITH THROUGH-SUBSTRATE VIAS

This application is a continuation of patent application Ser. No. 12/889,650, entitled "Noise Decoupling Structure with Through-Substrate Vias," filed on Sep. 24, 2010, which application is incorporated herein by reference.

BACKGROUND

Recent advances in the radio frequency (RF) device design and fabrication make possible the integration of high-frequency RF device in a three-dimensional (3D) structure. The use of the high-frequency RF devices causes severe noise coupling between devices. For example, analog circuits such as differential amplifiers are extremely sensitive to the noise at the differential inputs, and hence are specially affected by the noise generated in the 3D structures. This significantly limits the performance of the circuits comprising high-frequency RF devices. Therefore, noise isolation structures are needed to prevent the noise coupling between devices. With the use of high-frequency RF devices, the requirement of preventing noise coupling becomes more demanding.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1**A, **1**B, and **1**C illustrate a cross-sectional view, a top view, and a perspective view, respectively, of a noise decoupling structure;

FIGS. **2**, **3**A and **4** are top views of noise decoupling structures in accordance with various alternative embodiments; and

FIG. **3**B illustrates a cross-sectional view of the structure shown in FIG. **3**A.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

A novel noise decoupling structure is provided in accordance with an embodiment. The variations and the operation of the embodiments are then discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. Throughout the description, a noise decoupling structure for isolating an n-type device, which is further formed in a p-well region, is used as an example. One skilled in the art will realize the noise decoupling structures of p-type devices by applying the teaching of the embodiments of the present disclosure.

FIGS. **1**A, **1**B, and **1**C illustrate a cross-sectional view, a top view, and a perspective view, respectively, of a noise decoupling structure. Referring to FIG. **1**A, the noise decoupling structure includes deep n-well region **22**, guard ring **26**, through substrate vias (TSVs) **50**, and metal plate **36**. Integrated circuit device **24** is formed adjacent front surface **20***a* of semiconductor substrate **20**. In an embodiment, semiconductor substrate **20** is a bulk substrate comprising a semiconductor material such as silicon, silicon germanium, or the like. In alternative embodiments, semiconductor substrate **20** has a semiconductor-on-insulator (SOI) structure comprising buried oxide layer **21** (illustrated using dotted lines) formed between an overlying semiconductor layer and an underlying semiconductor layer. In an embodiment, semiconductor substrate **20** is lightly doped with a p-type impurity, although it may also be of n-type.

Integrated circuit device **24** may be a metal-oxide-semiconductor (MOS) device, which may further be a radio-frequency (RF) MOS device suitable for being operated at a high frequency, for example, higher than about 1 GHz. In alternative embodiments, integrated circuit device **24** may be a MOS varactor, an inductor, a bipolar junction transistor, a diode, or the like. Integrated circuit device **24** may include a single device or a plurality of devices. Guard ring **26** is formed in substrate **20**, and may encircle (please also refer to FIG. **1**B) integrated circuit device **24**. In an embodiment, p-well region **28**, on which n-type MOS device **24** may be formed, is encircled by, and may contact, guard ring **26**. In which case, guard ring **26** is formed of an n-well region. Shallow trench isolation (STI) regions **30** may be formed in substrate **20**, and the depth of guard ring **26** is greater than the depth of STI regions **30**. Further, deep n-well region **22** is formed directly underlying, and may contact, p-well region **28**. Deep n-well region **22** may contact guard ring **26**, and forms an uncapped box along with guard ring **26**, with guard ring **26** forming the sides of the uncapped box, and deep n-well region **22** forming the bottom of the uncapped box.

Optionally, an additional guard ring **48**, which may also be an n-well region, is formed to encircle guard ring **26**. Guard ring **48** may also contact the underlying deep n-well region **22**, and is horizontally spaced apart from guard ring **26** by STI region **30**A, which also forms a ring encircling guard ring **26**. In an embodiment, p-well region **51** may be between guard rings **26** and **48**, and spaces guard rings **26** and **48** apart from each other. In an embodiment, guard rings **26** and **48** comprise upper portions laterally spaced apart by STI region **30**A, and bottom portions contacting with each other. In alternative embodiments, p-well region **51** exists under STI region **30**A, and is between and contacting guard rings **26** and **48**. Contact plugs **34** are formed over, and are electrically coupled to, guard rings **26** and **48**. Guard rings **26** and **48** may be grounded, for example, through contact plugs **34**.

Metal plate **36** is formed on the backside of substrate **20**, and may contact back surface **20***b* of substrate **20**. The size of metal plate **36** is great enough to overlap an entirety of integrated circuit device **24**, and may be even greater to extend to directly under, and vertically overlapping, an entirety of guard ring **26**. Further, if guard ring **48** is formed, metal plate **36** may also extend to directly under, and vertically overlapping, an entirety of guard ring **48**. Metal plate **36**, however, does not cover all of the backside of semiconductor substrate **20**. In an embodiment, metal plate **36** is formed of copper, aluminum, silver, and/or the like.

Through substrate vias (TSVs) **50** are formed adjacent integrated circuit device **24**, and extend from the top surface **20***a* to back surface **20***b* of substrate **20**. TSVs **50** contact, and are electrically coupled to, metal plate **36**, which may be grounded. In an embodiment, only one TSV **50** is formed. In alternative embodiments, a plurality of TSVs **50** are formed, and may be distributed substantially uniformly through four sides surrounding integrated circuit device **24** (refer to FIG. **1**B and FIGS. **2** through **4**). TSVs **50** may penetrate through STI region **30**A, and possibly penetrates deep n-well region **22**. Further, if guard rings **26** and/or **48** extend to directly under STI region **30**A, TSVs **50** may also penetrate through

guard rings **26** and/or **48**. TSVs **50** may also be grounded, for example, through contact plugs **34**.

FIG. **1**B illustrates a top view of the structure shown in FIG. **1**A, which illustrated that guard rings **26** and **48** are formed to encircle integrated circuit device **24**. Further, TSVs **50** may be formed outside or inside guard ring **26**. TSVs **50** may be aligned to a rectangle, with TSVs **50** allocated along each side of the rectangle.

FIG. **1**C illustrates a perspective view of the structure shown in FIGS. **1**A and **1**B. An interconnect structure including metal lines **52** and vias **54**, which are electrically coupled to TSVs **50** and integrated circuit device **24**, is also illustrated. The portions of metal lines **52** and vias **54** that are electrically coupled to TSVs **50** may extend to upper metal layers such as the bottom metal layer (M**1**), the second metal layer (M**2**), the third metal layer (M**3**), the fourth metal layer (M**4**), and the overlying metal layers (not shown).

FIGS. **2** and **3**A illustrate the top views of alternative embodiments, in which only one guard ring is formed to encircle integrated circuit device **24**. FIG. **3**B illustrates a cross-sectional view of the structure shown in FIG. **3**A. Referring to FIG. **2**, TSVs **50** are formed inside guard ring **26**. Similar to the embodiment shown in FIGS. **1**A through **1**C, in these embodiments, TSVs **50** are formed outside the active region of integrated circuit **24** if it comprises a MOS device(s) or a MOS varactor(s). In FIG. **3**A, TSVs **50** are formed outside guard ring **26**. In each of the embodiments as shown in FIGS. **2** and **3**A/**3**B, deep n-well region **22** (not shown in FIGS. **2** and **3**A, please refer to FIGS. **1**A and **3**B) may be formed directly underlying integrated circuit device **24**, and may extend to directly underlying STI region **30**A and guard ring **26**. In the embodiment shown in FIG. **2**, TSVs **50** may also penetrate through the underlying deep n-well region **22**. Alternatively, as shown in FIG. **3**B, deep n-well region **22** does not extend to TSVs **50**, and hence TSVs **50** do not penetrate through deep n-well region **22**.

As also shown in FIGS. **2** and **3**A, TSVs **50** may be allocated to each of the four sides of a rectangular region surrounding device **24**, and may be aligned to one or more than one rectangles. For example, in FIGS. **2** and **3**A, TSVs **50** are aligned to the four sides of rectangles **53**A and **53**B.

FIG. **4** illustrates yet another embodiment, wherein no guard ring is formed. However, TSVs **50** are still formed, and are electrically coupled to underlying metal plate **36** (not shown in FIG. **4**, please refer to FIG. **1**A), which is directly underlying, and vertically overlapping, integrated circuit device **24**.

Although the discussed embodiments provide a method of forming a noise decoupling structure for an n-type MOS device, one skilled in the art will realize that the teaching provided is readily available for the formation of noise decoupling structures for p-type MOS devices, with the conductivity types of the respective well regions and guard rings inverted.

By forming metal plate **36** on the backside of the respective substrate, and by grounding the metal plate, integrated circuits may, in addition to be isolated by guard rings and deep well regions, also be isolated from noise by the underlying metal plates. The metal plates may collect the electrons leaked from devices, and hence the signal coupling in the vertical direction, particularly in three-dimensional (3D) structures, is prevented. Accordingly, better signal isolation may be achieved.

In accordance with embodiments, a device includes a substrate having a front surface and a back surface; an integrated circuit device at the front surface of the substrate; and a metal plate on the back surface of the substrate, wherein the metal plate overlaps substantially an entirety of the integrated circuit device. A guard ring extends into the substrate and encircles the integrated circuit device. The guard ring is formed of a conductive material. A TSV penetrates through the substrate and electrically couples to the metal plate.

In accordance with other embodiments, a semiconductor substrate includes a front surface and a back surface; an integrated circuit device at the front surface of the substrate; a metal plate on the back surface of the substrate, wherein the metal plate overlaps substantially an entirety of the integrated circuit device; a guard ring extending into the substrate and encircling the integrated circuit device, wherein the guard ring is formed of a first well region; a deep well region directly underlying the integrated circuit device and contacting the guard ring, wherein the guard ring and the deep well region are of a same conductivity type; and a TSV penetrating through the substrate and the deep well region, and electrically coupled to the metal plate.

In accordance with yet other embodiments, a device includes a p-type semiconductor substrate; a deep n-well region in the semiconductor substrate; a p-well region over and contacting the deep well region; a guard ring formed of an n-well region in the p-type semiconductor substrate and encircling the p-well region, wherein the guard ring extends from a front surface of the p-type semiconductor substrate into the p-type semiconductor substrate, and wherein the guard ring contacts the deep n-well region; a metal plate contacting a back surface of the semiconductor substrate; and a TSV penetrating through the p-type semiconductor substrate and contacting the metal plate.

Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A method comprising:

forming a first guard ring around a circuit region on a first side of a substrate, the first guard ring comprising a doped region of the substrate, the first guard ring having a first conductivity type, the circuit region having a second conductivity type;

forming a first isolation trench around the circuit region on the first side of the substrate;

forming through vias, the through vias extending through the first isolation trench to a second side of the substrate;

forming a second guard ring encircling the first guard ring, wherein the through vias are laterally between the first guard ring and the second guard ring, the second guard ring having the first conductivity type; and

forming a conductive layer over the second side of the substrate, the conductive layer being electrically coupled to the through vias, the conductive layer being over substantially an entirety of the second side of the substrate opposite of the circuit region.

2. The method of claim **1**, wherein the first guard ring is interposed between the through vias and the circuit region.

3. The method of claim **1**, further comprising forming a well region, wherein the first guard ring and the second guard ring are separated by the well region, the well region having the second conductivity type.

4. The method of claim **3**, wherein the through vias extend through the well region.

5. The method of claim **1**, further comprising forming a deep well region directly underlying the circuit region, the deep well region having the first conductivity type, the first guard ring contacting the deep well region.

6. The method of claim **1**, further comprising:

forming a deep well region directly underlying the circuit region, the first guard ring and the second guard ring contacting the deep well region, the deep well region having the first conductivity type.

7. The method of claim **1**, wherein the through vias are laterally between the circuit region and the first guard ring.

8. The method of claim **1**, further comprising forming a second isolation trench around the circuit region on the first side of the substrate, the first guard ring being interposed between the through vias and the second isolation trench.

9. A method comprising:

forming active devices in an active device region on a first side of a substrate, the substrate in the active device region having a first conductivity type;

forming a first isolation trench around the active devices on the first side of the substrate;

forming a first guard ring around the active devices, the first guard ring having a second conductivity type;

forming through substrate vias extending from the first side of the substrate to a second side of the substrate, the through vias extending through the first isolation trench, the through vias arranged in a pattern surrounding the active device region;

forming a second guard ring, wherein the first guard ring is interposed between the second guard ring and the active device region, and wherein the through vias are interposed between the first guard ring and the second guard ring, the second guard ring having the second conductivity type; and

forming a conductive layer over the second side of the substrate, the conductive layer being electrically coupled to the through vias, the conductive layer extending from a first through via to a second through via, wherein the active device region is interposed between the first through via and the second through via.

10. The method of claim **9**, further comprising forming a well of the first conductivity type directly below the first isolation trench, the well abutting the first guard ring.

11. The method of claim **9**, further comprising forming a well region, wherein the first guard ring and the second guard ring are separated by the well region, the well region having the first conductivity type.

12. The method of claim **11**, wherein the through vias extend through the well region.

13. The method of claim **9**, further comprising forming a deep well region directly underlying the active device region, the deep well region having the second conductivity type, the first guard ring contacting the deep well region.

14. The method of claim **9**, further comprising:

forming a deep well region directly underlying the active device region, the first guard ring and the second guard ring contacting the deep well region, the deep well region having the second conductivity type.

15. The method of claim **9**, further comprising forming a second isolation trench around the active devices on the first side of the substrate, the second isolation trench being interposed between the first guard ring and the active device region.

16. A method comprising:

forming a first isolation trench and a second isolation trench around a circuit region on a first side of a substrate, the circuit region having a first well, the first well having a first conductivity type;

forming a first guard ring around the circuit region, the first guard ring having a second conductivity type, at least a portion of the first guard ring being interposed between the first isolation trench and the second isolation trench, a bottom surface of the first guard ring being below a bottom of the first isolation trench and a bottom of the second isolation trench;

forming through vias extending through the first isolation trench; and

forming a conductive plate over a second side of the substrate, the conductive plate being electrically coupled to the through vias, the conductive plate covering a portion of the second side of the substrate opposing the circuit region.

17. The method of claim **16**, further comprising electrically coupling the first guard ring and the through vias to ground.

18. The method of claim **16**, further comprising a second guard ring, the through vias being interposed between the first guard ring and the second guard ring.

19. The method of claim **18**, further comprising forming a second well of the first conductivity type, wherein the second well is interposed between the first guard ring and the second guard ring.

20. The method of claim **19**, wherein the forming through vias comprises forming the through vias extending through the second well.

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